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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/519,144

12/27/2004

Yutaka Iguchi

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EXAMINER

GETACHEW, ABIY

ART UNIT

PAPER NUMBER

2841

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/519,144

Applicant(s)

IGUCHI, YUTAKA

Examiner

Abiy Getachew

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/27/04, 11/20/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakata (US 6,900,989 B2).

Regarding claim 1, Sakata discloses a chip on film carrier tape (20) including a continuous insulating film (12), a wiring pattern formed (21) of a conductor layer (11) provided on a surface of the insulating film (12), and a row of sprocket holes (22) provided on either lateral side of the wiring pattern (21) on which electronic devices are to be mounted [Column 9 paragraph 2 lines 7-21], characterized in that a center section of the insulating layer (21) other than opposite longitudinal edges where the sprocket holes (22) (See figure 2b) are formed is provided with a support film formed on another surface of the insulating film (12), which surface is opposite to the surface on which the wiring pattern (21) is provided.

Regarding claim 2, as applied claim 2 above Sakata discloses, wherein the row of sprocket holes (22) are provided with a dummy-wiring portion (12, i.e. Insulation is

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sometimes confused with either weatherization or thermal mass, but is distinct from both) surrounding the holes.

Regarding claim 3, as applied claim 2 above Sakata discloses, wherein the dummy-wiring portion (12, i.e. Insulation is sometimes confused with either weatherization or thermal mass, but is distinct from both) is provided in the form of discrete islands each surrounding a sprocket hole (22).

Regarding claim 4, as applied claim 3 above Sakata discloses, wherein the tape (20) has a predetermined distance between a longitudinal edge of the insulating layer (12) and a longitudinal edge of the dummy-wiring (12) portion. [Column 10 paragraph 4 lines 54-67]

Regarding claim 5, as applied claim 1 above Sakata discloses, wherein the support film has a thickness, which is equal to or less than that of the insulating layer (12). [Column 8 paragraph 3 and 4, lines 38-55]

Regarding claim 6, as applied claim 2 above Sakata discloses, wherein the support film (20) has a thickness, which is equal to or less than that of the insulating layer (12). [Column 8 paragraph 3 and 4, lines 38-55]

Regarding claim 7, as applied claim 3 above Sakata discloses, COF film carrier tape according to claim 3, where the support film has a thickness which is equal to or less than that of the insulating layer (12). [Column 8 paragraph 3 and 4, lines 38-55] (See example 5a-5e)

Regarding claim 8, as applied claim 4 above Sakata discloses, film carrier tape (20) according to claim 4 wherein the support. (See table 4)

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Regarding claim 9, as applied claim 5 above Sakata discloses, COF film carrier tape according to claim 5, (20) wherein the support film has a thickness of 25 to 50 micrometer. [Column 10 paragraph 3 lines 25-53]

Regarding claim 10, as applied claim 6 above Sakata discloses, wherein the support film (20) has a thickness of 25 to 50 micrometer. [Column 10 paragraph 3 lines 25-53]

Regarding claim 11, as applied claim 7 above Sakata discloses, wherein the support film (20) has a thickness of 25 to 50 micrometer. [Column 10 paragraph 3 lines 25-53]

Regarding claim 12, as applied claim 8 above Sakata discloses, wherein the support film (20) has a thickness of 25 to 50 micrometer. [Column 10 paragraph 3 lines 25-53]

Regarding claim 13, as applied claim 8 above Sakata discloses a method for producing a chip on film carrier tape (20) according to claim 1 including a continuous insulating film (12), a wiring pattern (21) formed of a conductor layer (11) provided on a surface of the insulating film (12), and a row of sprocket holes (22) provided on either lateral side of the wiring pattern (21) on which electronic devices are to be mounted [Column 9 paragraph 2 lines 7-21], characterized in that the method comprises a step of attaching a support film to a center section of the insulating layer (12) other than opposite longitudinal edges where the sprocket holes (12) are to be formed, the support film being formed on another surface of the insulating film (12), which surface is opposite to the surface on which the wiring pattern is provided a step of forming the

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sprocket holes in the opposite longitudinal edges; and a step of forming the wiring pattern (21) as well as a dummy wiring portion (element 12, i.e. Insulation is sometimes confused with either weatherization or thermal mass, but is distinct from both) surrounding the row of sprocket holes (22) by forming a resist pattern on the conductor layer and etching the conductor layer (11).

Regarding claim 14, as applied claim 13 above Sakata discloses wherein the dummy-wiring portion (12, i.e. Insulation is sometimes confused with either weatherization or thermal mass, but is distinct from both) is provided in the form of discrete islands each surrounding a sprocket hole (22).

Regarding claim 15, as applied claim 13 above Sakata discloses wherein the method further comprises, after formation of the dummy wiring portion (Element 12, i.e. Insulation is sometimes confused with either weatherization or thermal mass, but is distinct from both) a step of peeling off the support film (20).

Regarding claim 16, as applied claim 14 above Sakata discloses, wherein the method further comprises, after formation of the dummy wiring portion (element 12, i.e. Insulation is sometimes confused with either weatherization or thermal mass, but is distinct from both), a step of peeling off the support film (20).

Response to Arguments

3. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abiy Getachew whose telephone number is (571) 272 6932. The examiner can normally be reached on Monday to Friday 8Am to 4:30Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



TUAN T. DINH
PRIMARY EXAMINER

Abiy Getachew
Examiner
Art Unit 2841

A.G.
July 31, 2007